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09/578,895	05/26/2000	Shunpei Yamazaki	0756-2160	8423

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EXAMINER	
GEBREMARIAM, SAMUEL A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/578,895	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	SAMUEL A. GEBREMARIAM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) *17-23,25-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,29-31,33-36,38,39,41,42,44-47,49,50,52,53 and 55-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/19/09;5/8/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-10,17-23,25-27,29-31,33-36,38,39,41,42,44-47,49,50,52,53 and 55-64.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1, 5, 33 and 44 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/980,603 (603).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding claim 1, (603) teaches (claim 1) an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor (603, teaches a switching TFT and current-control TFT and both inherently have a gate electrode); and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the second thin film transistor, and wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor has two TFTs and hence two channel regions), at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed

between the channel regions (TFTs inherently have source and drain region, hence impurity regions).

Regarding claim 5, (603) teaches the entire claimed structure of claim 1 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (refer to claim 1).

Regarding claim 33, (603) teaches (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising an active layer and at least first and second gate electrodes (two TFTs inherently have two gate electrodes) adjacent to the active layer with a gate insulating film interposed therebetween; a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the current control element (refer to claim 1).

Regarding claim 44, (603) teaches (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising at least two thin film transistors; a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element electrically connected to the current control element.

3. Claims 1, 5, 8, 33, 35 and 44 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No.10/337,391 (391).

Regarding claim 1, (391) teaches (claim 1) an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor (603, teaches a switching TFT and current-control TFT and both inherently have a gate electrode); and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the second thin film transistor, and, wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor has two TFTs and hence two channel regions), at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions (LDD regions).

Regarding claim 5, (391) teaches the entire claimed structure of claim 1 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (refer to claim 1).

Regarding claim 8, (391) teaches the entire claimed structure of claim 1 above including wherein each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and one of a drain region or the

impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap the gate electrodes of the first thin film transistor and wherein the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly (refer to claim 1).

Regarding claim 29, (391) teaches (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the second thin film transistor, wherein the first thin film transistor comprises an active layer in which at least two channel regions connected in series are formed with an impurity region interposed therebetween, and wherein each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and one of a impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap a gate electrode of the first thin film transistor and wherein the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly.

Regarding claim 30, (391) teaches substantially the entire claimed structure of claims 2 and 3 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (claim 1).

Regarding claims 33 and 35, (391) teaches (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising an active layer and at least first and second gate electrodes (two TFTs inherently have two gate electrodes) adjacent to the active layer with a gate insulating film interposed therebetween; a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected the current control element (refer to claim 1).

Regarding claim 41, (391) teaches (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising an active layer and at least first and second gate electrodes adjacent to a the active layer with a gate insulating film interposed therebetween; a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the current control element, wherein each of the switching element and the current control element has at least one lightly doped impurity region where, wherein the lightly doped impurity region of the switching element does not overlap a gate electrode of the switching element and wherein the lightly doped impurity region of the current control element overlaps a gate electrode of the current control element at least partly.

Regarding claims 44, 46 and 52, (391) teaches (claim 1) the entire claimed structure of claim 41 above including an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising at least two thin film transistors; a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the current control element.

4. Claims 1-10, 29-31, 33-36, 38-39, 41-42, 44-47, 49-50, 52-53 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 17-30 of copending Application No.11/258,933 (933).

Regarding claims 1-10, 29-30, 33-35, 38, 41-42, 44-46, 49 and 52 (933) teaches (claims 1-10) an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the second thin film transistor, and wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor has two TFTs and hence two channel regions), at least two gate electrodes corresponding to the

channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions (LDD regions). Furthermore (933) teaches that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of W2/L2> 5×W1/L1 establishes where a channel length of the second thin film transistor is L2 (0.1-50μm), a channel width of the second thin film transistor is W2 (0.5 to 30μm), a channel length of the first thin film transistor is L1 (0.2 to 18μm) and a sum of each of lengths of the channel regions of the width of the first thin film transistor is W1 (0.1 to 5μm) (claim 3). In addition (933) teaches (claims 5-10) a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element electrically connected to the current control element, wherein each of the switching element and the current control element has at least one lightly doped impurity region where, wherein the lightly doped impurity region of the switching element does not overlap a gate electrode of the switching element and the lightly doped impurity region of the current control element overlaps a gate electrode of the current control element at least partly. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of pixels in the structure of (933), in order to form a functional display device. Furthermore (933) teaches substantially the entire claimed structure of claims 29, 33, 41, 44, 49 and 52 above including the substrate comprises a material selected from the group consisting of a glass, a glass ceramic, a quartz, a silicon, a ceramic, a metal, and a plastic (refer to claim 22 and 29).

5. Claims 2-4, 34, 38-39, 45, 49 and 50 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No. 10/980,603 (603) in view of Luo, US patent No., 4,040,073.

Regarding claims 2, 3-4, 9-10, 34, 38, 45 and 49 (603) teaches substantially the entire claimed structure of claim 1 except explicitly stating that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of W2/L2> 5×W1/L1 establishes where a channel length of the second thin film transistor is L2 (0.1-50μm), a channel width of the second thin film transistor is W2 (0.5 to 30μm), a channel length of the first thin film transistor is L1 (0.2 to 18μm) and a channel width of the first thin film transistor is W1 (0.1 to 5μm).

Luo teaches a switching thin film transistor T1 and a current control TFT T2, where the channel width can be adjusted depending on the function of the device (col. 3, lines 45-55).

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to adjust a channel width of the second thin film transistor and a channel width of the first thin film transistor as claimed as taught by Luo in the structure of (603) in order to form a device with improved stability (col. 2, lines 16-25).

Furthermore parameters such as channel length and channel width in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the channel length and channel width as claimed in the structure of (603) in order to form a device with improved stability (col. 2, lines 16-25).

Regarding claims 6 and 7, (603) teaches substantially the entire claimed structure of claims 2 and 3 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (claim 1).

Regarding claims 39 and 50, (603) teaches substantially the entire claimed structure of claims 2-3, 38 and 49 above including the substrate is glass (12, fig. 1, Luo).

6. Claims 2-4, 31, 34, 36, 38-39, 42, 45, 47, 49, 50 and 53 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No. 10/337,391 (391) in view of Luo, US patent No., 4,040,073.

Regarding claims 2, 3-4, 9-10, 34, 38, 45 and 49 (391) teaches substantially the entire claimed structure of claims 1 except explicitly stating that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of W2/L2> 5×W1/L1 establishes where a channel length of the second thin film transistor is L2 (0.1-50μm), a channel width of the second thin film

transistor is W2 (0.5 to 30μm), a channel length of the first thin film transistor is L1 (0.2 to 18μm) and a channel width of the first thin film transistor is W1 (0.1 to 5μm).

Luo teaches a switching thin film transistor T1 and a current control TFT T2, where the channel width can be adjusted depending on the function of the device (col. 3, lines 45-55).

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to adjust a channel width of the second thin film transistor and a channel width of the first thin film transistor as claimed as taught by Luo in the structure of (391) in order to form a device with improved stability (col. 2, lines 16-25).

Furthermore parameters such as channel length and channel width in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the channel length and channel width as claimed in the structure of (391) in order to form a device with improved stability (col. 2, lines 16-25).

Regarding claims 6 and 7, (391) teaches substantially the entire claimed structure of claims 2 and 3 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (claim 1).

Regarding claims 9 and 10, (391) teaches substantially the entire claimed structure of claims 2 and 3 above including wherein each of the first and second thin

film transistors has at least one lightly doped impurity region between a channel region and one of a drain region or the impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap a gate electrode of the first thin film transistor and the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly (refer to claim 1).

Regarding claims 31, 36, 42, 47, 50 and 53, (391) teaches substantially the entire claimed structure of claims 29, 33, 41, 44, 49 and 52 above except explicitly stating that the wherein the substrate comprises a material selected from the group consisting of a glass, a glass ceramic, a quartz, a silicon, a ceramic, a metal, and a plastic.

Luo teaches an electroluminescence device that is based on a glass substrate (12) in order to form a device with improved stability.

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to form the electroluminescence device of (391) on a glass substrate as taught by Luo in order to form a device with improved stability.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 5, 33 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa, US 6,194,837 in view of Kunii et al, US 5,412,493.

Regarding claim 1, Ozawa teaches (figs. 1-4 and 6) an electroluminescence display device comprising: a substrate (10); and a plurality of pixels (fig. 1) over the substrate, each of the plurality of pixels comprising: a first thin film transistor (20); a second thin film transistor (30) comprising a gate electrode electrically connected to the first thin film transistor (refer to fig. 2); and an electroluminescence element (40) electrically connected to the second thin film transistor (fig. 6), wherein the first thin film transistor comprises a channel regions in an active layer, a gate electrode corresponding to the channel region, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel region (inherent structural characteristics of a transistor structure).

Ozawa does not explicitly teach that the first thin film transistor comprises at least two channel regions in an active layer, at least two gate electrode corresponding to the channel regions.

Kunii teaches (fig. 1) a display device with a plurality of thin film transistor comprising at least two channel regions in an active layer, at least two gate electrode corresponding to the channel regions structure consisting of switching element for driving a picture element (col. 6, lines 39-67).

It would have been obvious to one of ordinary in the art at the time the invention was made to incorporate thin film transistor comprising at least two channel regions in an active layer, at least two gate electrodes corresponding to the channel regions as

taught by Kunii in the structure of Ozawa in order to provide a switching element for driving a picture element.

Regarding claim 5, Ozawa teaches substantially the entire claimed structure of claim 1 above including the first thin film transistor (fig. 1, of Kunii) is a switching thin film transistor and the second thin film (30 of Ozawa) transistor is a current control thin film transistor (refer to fig. 6).

Regarding claims 33 and 44, Ozawa teaches (figs. 1-4 and 6) an electroluminescence display device comprising: a substrate (10); and a plurality of pixels (7, fig. 3) over the substrate, each of the plurality of pixels comprising: a switching element (col. 6, lines 1-23) comprising an active layer and a gate electrode (21) adjacent to the active layer with a gate insulating film interposed therebetween; a current control element (30) comprising a gate electrode (31) electrically connected to the switching element (refer to fig. 2); and an electroluminescence element (40) electrically connected to the current control element (refer to fig. 6A).

Ozawa does not explicitly teach that the switching element comprising at least first and second gate electrodes adjacent to the active layer an active layer.

Kunii teaches (fig. 1) a display device with a plurality of thin film transistor comprising at least two channel regions in an active layer, at least two gate electrode corresponding to the channel regions structure consisting of switching element for driving a picture element (col. 6, lines 39-67).

It would have been obvious to one of ordinary in the art at the time the invention was made to incorporate the switching element comprising at least two channel regions

in an active layer, at least two gate electrodes corresponding to the channel regions as taught by Kunii in the structure of Ozawa in order to provide a switching element for driving a picture element.

9. Claims 2, 3-4, 6-7, 34, 38, 45, 49 and 55-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa in view of Kunii and in further view Luo.

Regarding claims 2, 3-4, 6-7, 34, 38, 45 and 49 Ozawa teaches substantially the entire claimed structure of claims 1 and 5 except explicitly stating that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of W2/L2> 5×W1/L1 establishes where a channel length of the second thin film transistor is L2 (0.1-50μm), a channel width of the second thin film transistor is W2 (0.5 to 30μm), a channel length of the first thin film transistor is L1 (0.2 to 18μm) and a channel width of the first thin film transistor is W1 (0.1 to 5μm).

Luo teaches a switching thin film transistor T1 and a current control TFT T2, where the channel width can be adjusted depending on the function of the device (col. 3, lines 45-55).

It would have been have obvious to one of ordinary skill in the art at the time the invention was made to adjust a channel width of the second thin film transistor and a channel width of the first thin film transistor as claimed as taught by Luo in the structure of Sasaki in order to form a device with improved stability (col. 2, lines 16-25).

Furthermore parameters such as channel length and channel width in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the channel length and channel width as claimed in the structure of Sasaki in order to form a device with improved stability (col. 2, lines 16-25).

Regarding claims 8-10, 35, 41, 46 and 52 Ozawa teaches substantially the entire claimed structure of claims 1-3, 33 and 44 above including each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and one of a drain region or the impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap a gate electrode of the first thin film transistor and the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly (refer to figs. 4 and 6a of Ozawa and fig. 1 of Kunii).

Regarding claims 29-30, Ozawa teaches substantially the entire claimed structure of claims 1-3 and 8-10 including the first thin film transistor is a switching thin film transistor (fig. 1, Kunii) and the second thin film transistor (30, Ozawa) is a current control thin film transistor.

Regarding claims 31, 36, 42, 47, 50 and 53, Ozawa teaches substantially the entire claimed structure of claims 29, 33, 41, 44, 49 and 52 above including the substrate is quartz (col. 6, line 48, Kunii).

Regarding claims 55-64, Sasaki teaches substantially the entire claimed structure of claims 29, 33, 41, 44, 49 and 52 above including the entire top surface of the active layer and impurity region is in contact with the gate insulating film (refer for example fig. 4, where the impurity regions 23 are in contact with the gate insulating film 50. Note, for a functioning device the top surface of the active region/impurity region has to be connected to an interconnect structure for integration purposes).

Response to Arguments

10. Applicant's arguments with respect to claims 1-10, 29-31, 33-36, 38-39, 41-42, 44-47, 49-50, 52-53 and 55-64 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAMUEL A. GEBREMARIAM whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-167070. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Samuel A Gebremariam/

Examiner, Art Unit 2811

/SAG/

July 18, 2009